Examples 5 and 6 because the copper powder was completely integrated with the conductor layer.

Industrial Applicability

As described above, the printed wiring board according to the present invention is useful for a multilayer wiring board which is used as a packaging substrate for packing IC chips, in particular for a multilayer printed wiring board obtained by a semi-additive process or a full-additive process. In addition, the resin composition according to the present invention is applicable as through-holes, as well as an interlaminar insulating resin layer of a printed wiring board.

What is claimed is:

1. A multilayer printed wiring board comprising a substrate provided with at least one through-hole, the substrate having at least one interlaminar resin insulating layer formed thereon and at least one conductor circuit formed on the at least one interlaminar resin insulating layer, the at least one through-hole being filled with filler, wherein

an internal surface of the at least one through-hole is roughened, and the filler comprises metal particles and one of thermosetting and thermoplastic resin.

2. The multilayer printed wiring board according to claim 1, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least one prepreg in alternating order.

3. The multilayer printed wiring board according to claim 1, wherein at least one through-hole formed on the substrate has a pitch interval of equal to or less than 700 μm.

4. The multilayer printed wiring board according to claim 1, comprising build-up wiring layers including at least one via-hole provided in the at least one interlaminar resin insulating layer wherein the build-up wiring layers are formed on both surfaces of the substrate, and have the same number of layers with each other.

5. A multilayer printed wiring board comprising a substrate provided with at least one through-hole, the substrate having at least one interlaminar resin insulating layer formed thereon and at least one conductor circuit formed on the at least one interlaminar resin insulating layer, the at least one through-hole being filled with filler, wherein

an internal surface of the at least one through-hole is roughened, and the filler comprises particulate substance having a particle size of from 0.1 to 30 μm, resin, and ultrafine inorganic powder having a particle size from 1 to 1000 nm.

6. The multilayer printed wiring board according to claim 5, wherein the filler is a nonconducting composition containing metal particles.

7. The multilayer printed wiring board according to claim 5, wherein the particulate substance comprises at least one of metal particles, inorganic particles and resin particles.

8. The multilayer printed wiring board according to claim 5, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

9. The multilayer printed wiring board according to claim 5, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least prepeg in alternating order.

10. The multilayer printed wiring board according to claim 5, wherein the at least one through-hole formed on the substrate has ahigh pitch interval of equal to or less than 700 μm.

11. The multilayer printed wiring board according to claim 5, comprising build-up wiring layers including at least one via-hole provided in the at least one interlaminar resin insulating layer wherein the build-up wiring layers are formed on both surfaces of the substrate, and have the same number of layers with each other.

12. A multilayer printed wiring board comprising a substrate provided with at least one through-hole, the substrate having at least one interlaminar resin insulating layer formed thereon and at least one conductor circuit formed on the at least one interlaminar resin insulating layer, the at least one through-hole being filled with filler, wherein

an internal surface of the at least one through-hole is roughened, and the filler comprises metal particles and one of thermosetting and thermoplastic resin, and an exposed portion of the filler in the at least one through-hole is covered with a portion of the at least one conductor circuit.

13. The multilayer printed wiring board according to claim 12, wherein a roughened layer is formed on a surface of the at least one conductor circuit covering at least the one through-hole.

14. The multilayer printed wiring board according to claim 12, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least one prepreg in alternating order.

15. The multilayer printed wiring board according to claim 12, wherein the at least one through-hole formed on the substrate has a pitch interval of equal to or less than 700 μm.

16. The multilayer printed wiring board according to claim 12, comprising build-up wiring layers including the at least one via-hole provided in the at least one interlaminar resin insulating layer wherein the build-up wiring layers are formed on both surfaces of the substrate, and have the same number of layers with each other.

17. A multilayer printed wiring board comprising a substrate provided with at least one through-hole, the substrate having at least one interlaminar resin insulating layer formed thereon and at least one conductor circuit formed on the at least one interlaminar resin insulating layer, the at least one through-hole being filled with filler, wherein

an internal surface of the at least one through-hole is roughened, and the filler comprises particulate substance having a particle size of from 0.1 to 30 μm, resin, and ultrafine inorganic powder having a particle size from 1 to 1000 nm, and an exposed portion of the filler in the at least one through-hole is covered with a portion of the at least one conductor circuit.

18. The multilayer printed wiring board according to claim 17, wherein the filler is a nonconducting composition containing metal particles.

19. The multilayer printed wiring board according to claim 17, wherein the particulate substance comprises at least one of metal particles, inorganic particles and resin particles.

20. The multilayer printed wiring board according to claim 17, wherein the resin comprises at least one of bisphenol epoxy resin ans novolac epoxy resin.

21. The multilayer printed wiring board according to claim 17, wherein the roughened layer is formed on a surface of the at least one conductor circuit covering the least one through-hole.

22. The multilayer printed wiring board according to claim 17, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least one prepreg in alternating order.

23. The multilayer printed wiring board according to claim 17, wherein at least one through-hole formed on the substrate has a pitch interval wqual to or less than 700 μm.

24. The multilayer printed wiring board according to claim 17, comprising build-up wiring layers including the at least one via-hole provided in the at least one interlaminar

resin insulating layer wherein the build-up wiring layers are formed on both surfaces of the substrate, and have the same number of layers with each other.

25. A multilayer printed wiring board comprising a substrate provided with at least one through-hole, the substrate having at least one interlaminar resin insulating layer formed thereon and at least one conductor circuit formed on the at least one interlaminar resin insulating layer, the at least one through-hole being filled with filler, wherein

an internal surface of the at least one through-hole is roughened, and the filler comprises metal particles and one of thermosetting and thermoplastic resin, and an exposed surface of the filler in the at least one through-hole is covered with a portion of the at least one conductor circuit, and at least one viahole is formed in the at least one interlaminar resin insulating layer just above the at least one conductor circuit and is connected to the at least one conductor circuit.

26. The multilayer printed wiring board according to claim 25, wherein a roughened layer is formed on the surface of the through-hole-covering conductor layer.

27. The multilayer printed wiring board according to claim 25, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least one prepreg in alternating order.

28. The multilayer printed wiring board according to claim 25, wherein the at least one through-hole formed on the substrate has a pitch interval of equal to or less than 700 μm.

29. The multilayer printed wiring board according to claim 25, comprising build-up wiring layers including the at least one via-hole provided in the at least one interlaminar resin insulating layer wherein the build-up wiring layers are formed on both surfaces of the substrate, and have the same number of layers with each other.

30. A multilayer printed wiring board comprising a substrate provided with at least one through-hole, the substrate having at least one interlaminar resin insulating layer formed thereon and at least one conductor circuit formed on the at least one interlaminar resin insulating layer, the at least one through-hole being filled with filler, wherein

an internal surface of the at least one through-hole is roughened, and the filler comprises particulate substance having a particle size of from 0.1 to 30 μm, resin, and ultrafine inorganic powder having a particle size from 1 to 1000 nm, and an exposed surface of the filler in the at least one through-hole is covered with a portion of the at least one conductor circuit, and at least one viahole is formed in the at least one interlaminar resin insulating layer just above the at least one conductor circuit and is connected to the at least one conductor circuit.

31. The multilayer printed wiring board according to claim 30, wherein the filler is a nonconducting composition containing metal particles.

32. The multilayer printed wiring board according to claim 30, wherein the particulate substance comprises at least one of metal particles, inorganic particles and resin particles.

33. The multilayer printed wiring board according to claim 30, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

34. The multilayer printed wiring board according to claim 30, wherein a roughened layer is formed on a surface of the at least one conductor circuit covering the at least one through-hole.

35. The multilayer printed wiring board according to claim 30, wherein the substrate is a multilayer core substrate formed by laminating at least one conductor layer and at least one prepreg in alternating order.

36. The multilayer printed wiring board according to claim 30, wherein the least one throhg-hole formed on the substrate has a pitch interval of equal to or less than 700 μm.

37. The multilayer printed wiring board according to claim 30, comprising build-up wiring layers including the at least one via-hole provided in the at least one interlaminar resin insulating layer wherein the build-up wiring layers are formed on both surfaces of the substrate, and have the same number of layers with each other.

38. A resin composition for filling through-hole of a printing wiring board comprising:

particulate substance comprising metal powder having an average particle size ranging from 0.1 to 30 μm and being present in an amount ranging from 30 to 90% by weight of the total solids content of the resin composition,

resin and

ultrafine inorganic powder having an average particle size ranging from 1 to 1,000 nm.

39. The resin composition according to claim 38, which is a nonconducting composition.

40. The resin compositon according to claim 38, wherein the particle substance comprises at least one member selected from metal particles, inorganic particles or resin particles.

41. The resin composition according to claim 38, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

42. The resin composition according to claim 41, wherein the bisphenol epoxy resin comprises at least one of bisphenol P epoxy resin and bisphenol A epoxy resin.

43. The resin composition according to claim 41, wherein the novalac epoxy resin comprises at least one of phenol novalac epoxy resin and cresol novalac epoxy resin.

44. The resin composition according to claim 41, wherein the composition ratio of the novalac epoxy resin to the bisphenol epoxy resin ranges from 1/1 to 1/100 by weight.

45. The resin composition according to claim 38, wherein the ultrafine inorganic powder is present in an amount ranging from 0.1 to 5% by weight of the total solids content of the resin composition and has an average particle size ranging from 2 to 200 nm.

46. The resin composition according to claim 38, wherein the ultrafine inorganic powder is selected from silica, alumina, silicon carbide or mullite.

47. The resin composition according to claim 46, wherein the ultrafine inorgainic powder is silica.

48. A process of producing a multilayer printed wiring board comprising:

forming at least one conductor layer on both surfaces of a substrate by electroless plating,

forming at least one through-hole on the substrate,

forming a roughened layer on an internal surface of the at least one through-hole,

filling the at least one through-hole having the roughened layer on its internal surface with filler comprising metal particles and one of thermosetting and thermoplastic resin, and drying and curing the filler,

forming at lest one interlaminar resin insulating layer, and

forming at least one conductor circuit by electroless plating.

49. The process according to claim 48, wherein the internal surface of the at least one through-hole is roughened by a treatment selected from an oxidation-reduction

treatment, a treatment with an aqueous mixed solution of an organic acid and a copper (II) complex, or a plating treatment with a needle ternary alloy of copper-nickel-phosphorous.

50. The process according to claim **48**, wherein forming the least one conductor layer comprises electroplating after electroless plating.

51. The process according to claim **48**, wherein forming the at least one conductor circuit comprises electroplating after electroless plating.

52. A process of producing a multilayer printed wiring board comprising:

forming at least one conductor layer on both surfaces of a substrate by electroless plating,

forming at least one through-hole through the substrate,

forming a roughened layer on an internal surface of the at least one through-hole,

filling the at least one through-hole having the roughened layer on its internal surface with filler comprising particulate substance having a particle size of from 0.1 to 30 μm, resin, and ultrafine inorganic powder having a particle size from 1 to 1000 nm, and drying and curing the filler,

forming at least one interlaminar resin insulating layer, and

forming at least one conductor circuit by electroless plating.

53. The process according to claim **52**, wherein the filler is a nonconducting composition containing metal particles.

54. The process according to claim **52**, wherein the particulate substance comprises at least one of metal particles, inorganic particles and resin particles.

55. The process according to claim **52**, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

56. The process according to claim **52**, wherein forming the at least one conductor layer comprises electroplating after electroless plating.

57. The process according to claim **52**, wherein forming the at least one conductor circuit comprises electroplatinng after electroless plating.

58. A process of producing a multilayer printed wiring board comprising:

forming at least one conductor layer on both surfaces of a substrate by electroless plating,

forming at least one through-hole on the substrate,

forming a roughened layer on an internal surface of the at lest one through-hole,

filling the at least one through-hole having the roughened layer on its internal surface with filler comprising metal particles and one of thermosetting and thermoplastic resin, and drying and curing the filler,

forming a portion of the at least one conductor layer on the at least one through-hole by subjecting a portion of the filler on the at least one through-hole to electroless plating,

forming at least one interlaminar resin insulating layer, and

forming at least one conductor circuit by electroless plating.

59. The process according to claim **58**, wherein the internal surface of the at least one through-hole is roughened by any process selected from an oxidation-reduction tretment, a treatment with an aqueous mixed solution of an organic acid and a copper (II) complex, or a plating treatment with a needle ternary alloy of copper-nickel-phosphorus.

60. The process according to claim **58**, wherein the forming the portion of the at least one conductor layer on the at least one through-hole comprises smoothing a surface of the substrate, applying catalyst nuclei to the smoothed surface of the substrate, subjecting the substrate to electroless plating to form a plating layer, forming an etching resist just above the at least one through-hole and on a portion of the at least one through-hole and the plating layer which is to become a part of the at least one conductor circuit, removing the plating layer in a portion of the substrate where the etching resist is not formed, and removing the etching resist.

61. The process according to claim **60**, comprising subjecting the substrate to electroplating after electroless plating.

62. The process according to claim **60**, wherein the forming the portion of the at least one conductor layer on the at least one through-hole comprises smoothing a surface of the substrate, forming a plating resist on a part of the smoothed surface of the substrate, subjecting a portion of the smoothed surface of the substrate where the resist is not formed to electroplating to form the at least one conductor layer and the at least one conductor circuit, and removing the plating resist with the at least one conductor layer located beneath the plating resist by etching.

63. The process according to claim **60**, wherein the forming the portion of the at least one conductor layer on the at least one through-hole comprises roughening a surface of the portion of the at least one conductor layer by a treatment selected from oxidation-reduction treatment, treatment with an aqueous mixed solution of an organic acid and a copper (II) complex, or plating treatment with needle ternary alloy of copper-nickel-phosphorus.

64. The process according to claim **60**, wherein forming the at least one conductor layer comprises electroplating after electroless plating.

65. The process according to claim **60**, wherein forming the portion of the at least one conductor layer on the at least one through-hole comprises electroplating after electroless plating.

66. A process of producing a multilayer printed wiring board comprising:

forming at least one conductor layer on both surfaces of a substrate by electroless plating,

forming at least one through-hole on the substrate,

forming a roughened layer on an internal surface of the at least one through-hole,

filling the at least one through-hole having the roughened layer on its internal surface with filler comprising particulate substance having a particle size of from 0.1 to 30 μm, resin, and ultrafine inorganic powder having a particle size from 1 to 1000 nm, and drying and curing the filler,

forming a portion of the at least one conductor layer on the at least one through-hole by subjecting a portion of the filler on the at least one through-hole to electroless plating,

forming at least one interlaminar resin insulating layer, and

forming at least one conductor circuit by electroless plating.

67. The process according to claim **66**, wherein the filler is a nonconducting composition having a specific resistance of equal to or more than 1×10^6 $\Omega\cdot cm^2$ and containing metal particles.

68. The process according to claim **67**, wherein the particulate substance comprises at least one of metal particles, inorganic particles and resin particles.

69. The process according to claim 67, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

70. The process according to claim 66, wherein forming the at least one conductor layer comprises electroplating after electroless plating.

71. The process according to claim 66, wherein forming the portion of the at least one conductor layer on the at least one through-hole comprises electroplating after electroless plating.

72. A process of producing a multilayer printed wiring board comprising:

forming at least one conductor layer on both surfaces of a substrate by electroless plating,

forming at least one through-hole on the substrate,

forming a roughened layer on an internal surface of the at least one through-hole,

filling the at least one through-hole having the roughened layer on its internal surface with filler comprising metal particles and one of the thermosetting and thermoplastic resin, and drying and curing the filler,

forming a portion of the at least one conductor layer on the at least one through-hole by subjecting a portion of the filler on the at least one through-hole to electroless plating,

forming at least one interlaminar resin insulating layer,

forming at least one viahole and at least one conductor circuit in the at least one interlaminar resin insulating layer located just above the at least one through-hole, and

connecting the at least one viahole to the at least one conductor circuit in the at least one interlaminar resin insulating layer located just above the at least one through-hole.

73. The process according to claim 72, wherein the internal surface of the at least one through-hole is roughened by a treatment selected from oxidation-reduction treatment, treatment with an aqueous mixed solution of an organic acid and a copper (II) complex, or plating treatment with needle ternary alloy of copper-nickel-phosphorus.

74. The process according to claim 72, wherein the forming the portion of the at least one conductor layer on the at least one through-hole comprises smoothing a surface of the substrate, applying catalyst nuclei to the smoothed surface of the substrate, subjecting the substrate to electroless plating to form a plating layer, forming an etching resist just above the at least one through-hole and on a portion of the at least one through-hole and the plating layer which is to become a part of the at least one conductor circuit, removing the plating layer in a portion of the substrate where the etching resist is not formed, and removing the etching resist.

75. The process according to claim 72, wherein the forming the portion of the at least one conductor layer on the at least one through-hole comprises smoothing a surface of the substrate, forming a plating resist on a part of the smoothed surface of the substrate, subjecting a portion of the smoothed surface of the substrate where the resist is not formed to electroplating to form the at least one conductor layer and the at least one conductor circuit, and removing the plating resist with the at least one conductor layer located beneath the plating resist by etching.

76. The process according to claim 72, wherein the forming the portion of the at least one conductor layer on the at least one through-hole comprises roughening a surface of the portion of the at least one conductor layer by a treatment selected from oxidation-reduction treatment, treatment with an aqueous mixed solution of an organic acid and a copper (II) complex, or plating treatment with needle ternary alloy of copper-nickel-phosphorus.

77. The process according to claim 72, wherein the at least one viahole is formed just above the at least one through-hole through the interposition of the at least one interlaminar resin insulating layer by roughening the at least one interlaminar resin insulating layer provided with an opening for the at least one viahole, applying catalyst nuclei directly to the roughened interlaminar resin insulating layer, subjecting the roughened interlaminar resin insulating layer to electroless plating, and etching the plated layer so as to leave the at least one viahole and the at least one conductor circuit portion.

78. The process according to claim 72, wherein the at least one viahole is formed just above the at least one through-hole through the interposition of the at least one interlaminar resin insulating layer by applying catalyst nuclei directly to the interlaminar resin insulating layer without roughening, subjecting the interlaminar resin insulating layer to electroless plating, and etching the plated layer so as to leave at least one viahole and the at least one conductor circuit portion.

79. The process according to claim 72, wherein forming at least one conductor layer on both surfaces of a substrate comprises electroplating after electroless plating.

80. The process according to claim 72, wherein forming a portion of the at least one conductor layer on the at least one through-hole comprises electroplating after electroless plating.

81. A process of producing a multilayer printed wiring board comprising:

forming at least one conductor layer on both surfaces of a substrate by electroless plating,

forming at least one through-hole on the substrate,

forming a roughened layer on an internal surface of the at least one through-hole,

filling the at least one through-hole having the roughened layer on its internal surface with filler comprising particulate substance having a particle size of from 0.1 to 30 μm, resin, and ultrafine inorganic powder having a particle size from 1 to 1000 nm, and drying and curing the filler,

forming a portion of the at least one conductor layer on the at least one through-hole by subjecting a portion of the filler on the at least one through-hole to electroless plating,

forming at least one interlaminar resin insulating layer,

forming at least one viahole and at least one conductor circuit in the at least one interlaminar resin insulating layer located just above the at least one through-hole, and

connecting the at least one viahole to the at least one conductor circuit located just above the at least one through-hole.

82. The process according to claim 81, wherein the filler is a nonconducting composition and further comprises metal particles.

83. The process according to claim 82, wherein the particulate substance comprises at least one of metal particles, inorganic particles and resin particles.

84. The process according to claim 82, wherein the resin comprises at least one of bisphenol epoxy resin and novolac epoxy resin.

85. The process according to claim 82, wherein forming the at least one conductor layer comprises electroplating after electroless plating.

86. The process according to claim 82, wherein forming the portion of the at least one conductor layer on the at least one through-hole comprises electroplating ater electroless plating.

87. A multilayer printed wiring board comprising:

a substrate having at least one through-hole which includes a roughened internal surface;

at least one interlaminar resin insulating layer which is provided on the substrate and in which at least one via hole is provided;

at least one conductor circuit provided on the interlaminar resin insulating layer;

filler provided in the through-hole; and

a through-hole-covering conductor layer provided to cover the filler provided in the through-hole, said at least one via hole being connected to said through-hole-covering conductor layer.

88. The multilayer printed wiring board according to Claim 87, wherein said via hole is filled with a plated film or a filler .

89. The multilayer printed wiring board according to Claim 87, wherein a roughened layer is provided on a surface of said through-hole-covering conductor layer.

90. The multilayer printed wiring board according to Claim 89, wherein the roughened layer is provided on a side face of said through-hole-covering conductor layer.

91. The multilayer printed wiring board according to Claim 87, further comprising:

a roughened layer provided in said at least one through-hole and having the roughened internal surface, a thickness of the roughened layer being at least 0.1 μm and at most 10 μm.

92. The multilayer printed wiring board according to Claim 87, wherein said substrate comprises a glass-epoxy substrate, a polyimide substrate, a bismaleimide-triazine resin substrate, a fluororesin substrate, a copper-clad laminate resin substrate, a ceramic substrate, or a metal substrate.

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